MSP430xG46x Demo - FLL+, LPM3 Using Basic Timer ISR, 32kHz ACLK

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; Description: System runs normally in LPM3 with basic timer clocked by

; 32kHz ACLK. At a 2 second interval the basic timer ISR will wake the

; system and flash the LED on P5.1 inside of the Mainloop.

; ACLK = LFXT1 = 32768Hz, MCLK = SMCLK = default DCO = 32 x ACLK = 1048576Hz

; //\* An external watch crystal between XIN & XOUT is required for ACLK \*//

;

; MSP430xG461x

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; /|\| XIN|-

; | | | 32kHz

; --|RST XOUT|-

; | |

; | P5.1|-->LED

;

; Texas Instruments Inc.

; Built with IAR Embedded Workbench Version: 3.41A

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#include <msp430xG46x.h>

;-------------------------------------------------------------------------------

RSEG CSTACK ; Define stack segment

;-------------------------------------------------------------------------------

RSEG CODE ; Assemble to Flash memory

;-----------------------------------------------------------------------------

RESET mov.w #SFE(CSTACK),SP ; Initialize stackpointer

StopWDT mov.w #WDTPW+WDTHOLD,&WDTCTL ; Stop WDT

SetupFLL bis.b #XCAP14PF,&FLL\_CTL0 ; Configure load caps

OFIFGcheck bic.b #OFIFG,&IFG1 ; Clear OFIFG

mov.w #047FFh,R15

OFIFGwait dec.w R15 ; Wait for OFIFG to set again if

jnz OFIFGwait ; not stable yet

bit.b #OFIFG,&IFG1 ; Has it set again?

jnz OFIFGcheck ; If so, wait some more

SetupBT ---------------------; Basic Timer1 Control Register. 2seconds

---------------- ; Enable Basic Timer interrupt

SetupPx ---------------- ; P6.x output

---------------- ; clear PORT6

---------------- ; P5.x output

---------------- ; clear PORT5

---------------- ; P4.x output

---------------- ; clear PORT4

---------------- ; P3.x output

---------------- ; clear PORT3

---------------- ; P2.x output

---------------- ; clear PORT2

---------------- ; P1.x output

---------------- ; clear PORT1

Mainloop ---------------- ; Enter LPM3, enable interrupts

---------------- ; Set P5.1

---------------- ; Push Delay 2000 to TOS

Pulse ---------------- ; Decrement Value at TOS

---------------- ; Delay done?

---------------- ; Increment destination twice

---------------- ; Reset P5.1

jmp Mainloop ;

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;------------------------------------------------------------------------------

BT\_ISR; Exit LPM3 on reti

;------------------------------------------------------------------------------

bic.w #LPM3,0(SP) ;

reti ;

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;-----------------------------------------------------------------------------

COMMON INTVEC ; Interrupt Vectors

;-----------------------------------------------------------------------------

ORG RESET\_VECTOR ; RESET Vector

DW RESET ;

ORG BASICTIMER\_VECTOR ; Basic Timer Vector

DW BT\_ISR ;

END